REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 9, 13, 16-17, 20 and 22 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Tanzawa et al.* (U.S. Patent No. 6,605,986). Claims 9, 13, 16-17 and 22 were also rejected under 35 U.S.C. § 102(e) as being anticipated by *Hirano* (U.S. Patent No. 6,747,901). Applicant respectfully traverses this rejection.

Claims 9, 13, 20, and 22 have been amended to more clearly claim the subject matter that Applicant regards as the invention. Claims 9, 13, and 22 have been amended to include limitations making it clear that there are multiple sets of wordlines each coupled to a different row decoder. These limitations are disclosed in the specification and drawings including Figure 4. Therefore, no new matter has been entered by this amendment.

Tanzawa et al. disclose a semiconductor memory device. Figure 1 shows a memory cell that is formed in a p-well 73 that is formed in an n-well 72 and both are formed in a p-substrate 71. Figure 2 shows a circuit of a memory cell array. Neither of these figures teach or suggest Applicant's invention as claimed in the amended claims.

The Examiner contends that Figure 1 shows a substrate of a second conductivity with a plurality of lower wells having a first conductivity with each lower well having an inner isolation well of the second conductivity. The Examiner further contends that Figure 2 shows a plurality of memory blocks, each memory block located in a different isolation well. However, these figures only show one isolation well within another well and a single memory cell within that inner well. Additionally, Figure 2 shows only a NOR memory cell array. There is no teaching or suggestion that any memory blocks formed within the memory array are located in different isolation wells as claimed in Applicant's amended claims. Further, there is no teaching or suggestion in *Tanzawa et al.* that each memory block is coupled to a first set of wordlines of a plurality of sets of wordlines as claimed by Applicant.

Hirano discloses a non-volatile semiconductor memory device. Figure 1 shows the memory device and Figure 2 shows an inner p-well within an n-well. However, there is no teaching or suggestion that each memory block of a plurality of memory blocks is located within a different isolation well as claimed in Applicant's amended claims. Further, there is no teaching

or suggestion in *Hirano* that each memory block is coupled to a first set of wordlines of a plurality of sets of wordlines. Hirano's teachings do not go beyond a single n-well with an inner p-well containing a plurality of memory cells.

Allowable Subject Matter

Claims 10-11, 14-15 and 21 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicant has amended claim 20 as suggested by the Examiner by including the limitations of claim 21. Claim 21 has been canceled to avoid duplication. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of the claims.

Claims 18-19 were allowed.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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Kenneth W. Bolvin
Reg. No. 34,125

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250